EXHIBIT C

Westlaw.
Not Reported in F.Supp.2d
2003 WL 360256 (D.Del.)
(Cite as: 2003 WL 360256 (D.Del.))

H

Motions, Pleadings and Filings

Only the Westlaw citation is currently available.

United States District Court,
D. Delaware.
INTEL CORPORATION, Plaintiff,
v.
BROADCOM CORPORATION, Defendant.
No. Civ.A. 00-796-SLR.

Feb. 13, 2003.

William J. Marsden, Jr., of Fish & Richardson, P.C., Wilmington, Delaware, John E. Gartman, and Juanita Brooks, of Fish & Richardson, P.C., San Diego, California, for Plaintiff, of counsel.

Richard H. Morse, and John W. Shaw, of Young Conaway Stargatt & Taylor, L.L.P., Wilmington, Delaware, Wilson Sonsini Goodrich & Rosati, P.C., Palo Alto, California. McDermott Will & Emery, Palo Alto, California. McDermott Will & Emery, Washington, D.C., for Defendant, of counsel.

OPINION

ROBINSON, Chief J.

I. INTRODUCTION

***1** On August 30, 2000, plaintiff Intel Corporation ("Intel") filed this action against defendant Broadcom Corporation ("Broadcom"), alleging infringement of certain claims of United States Patent Nos. 4,975,830 (the " '830 patent"), 4,823,201 (the " '201 patent"), 5,894,410 (the " '410 patent"), 5,079,630 (the " '630 patent") and 5,134,478 (the " '478 patent") (collectively, the "Intel patents"). The Intel patents cover three different technologies (smart networking products, semiconductor chip packaging structures, and digital video encoding and decoding techniques) that plaintiff alleges intersect in defendant's high-speed networking and communications products. The parties tried their claims regarding the '830 and '201 patents to a jury from November 28, 2001 to December 14, 2001. Currently before the court are the parties' motions for judgment as a matter of law and motions for a new trial.

II. BACKGROUND

A. The Patents in Suit

1. The '830 Patent

The '830 patent, entitled "Computer Communication System Having Supplemental Formats," issued on December 4, 1990. The named inventors are George E. Gerpheide, Kerry D. Sharp, Daniel J. Lee, David C. Olsen, David B. Meyer and Mark E. Kohagen. The listed assignee is Dayna Communication, Inc. Intel acquired the rights to the '830 patent when it acquired Dayna Communications.

The '830 patent discloses a communication system, such as a computer network, in which devices on the network (called nodes) can dynamically choose between multiple formats (e.g., various transmission characteristics including transmission speeds, encoding protocols, compression protocols, and encryption protocols) by which to transmit and receive data to and from one another over a common communication medium. Using the invention, a device on the network that seeks to transmit information can dynamically determine all of the formats by which it can communicate with a device that it wishes to send information. The optimal format that is supported by both devices is then selected and used to transmit information. In this way, when faster devices are added to a network they can dynamically communicate with each other using that fast format, but also communicate with slower devices using a slower format.

The invention, as described by the patent, works as follows. Each device on the network includes in its memory a list of its own transfer formats and the transfer formats that are supported by every other device on the network. These format sets are represented in memory by strings of bits. For example, a string of 001 would mean that the associated node does not support transfer format 1 or 2, but supports transfer format 3. When a device needs to transmit information to another device, it searches its memory for the supported format set of the destination device. If no format set is located for the device to which it wishes to send information, the transmitting device performs an inquiry dialog with the other device to learn and store the other device's

supported format set. Then, using algorithms that are applied through circuitry and software, it selects the optimal format which is mutually compatible with itself and the destination device. A flow chart of the logic used by the algorithm to select a transfer format is shown in Figure 4 below.

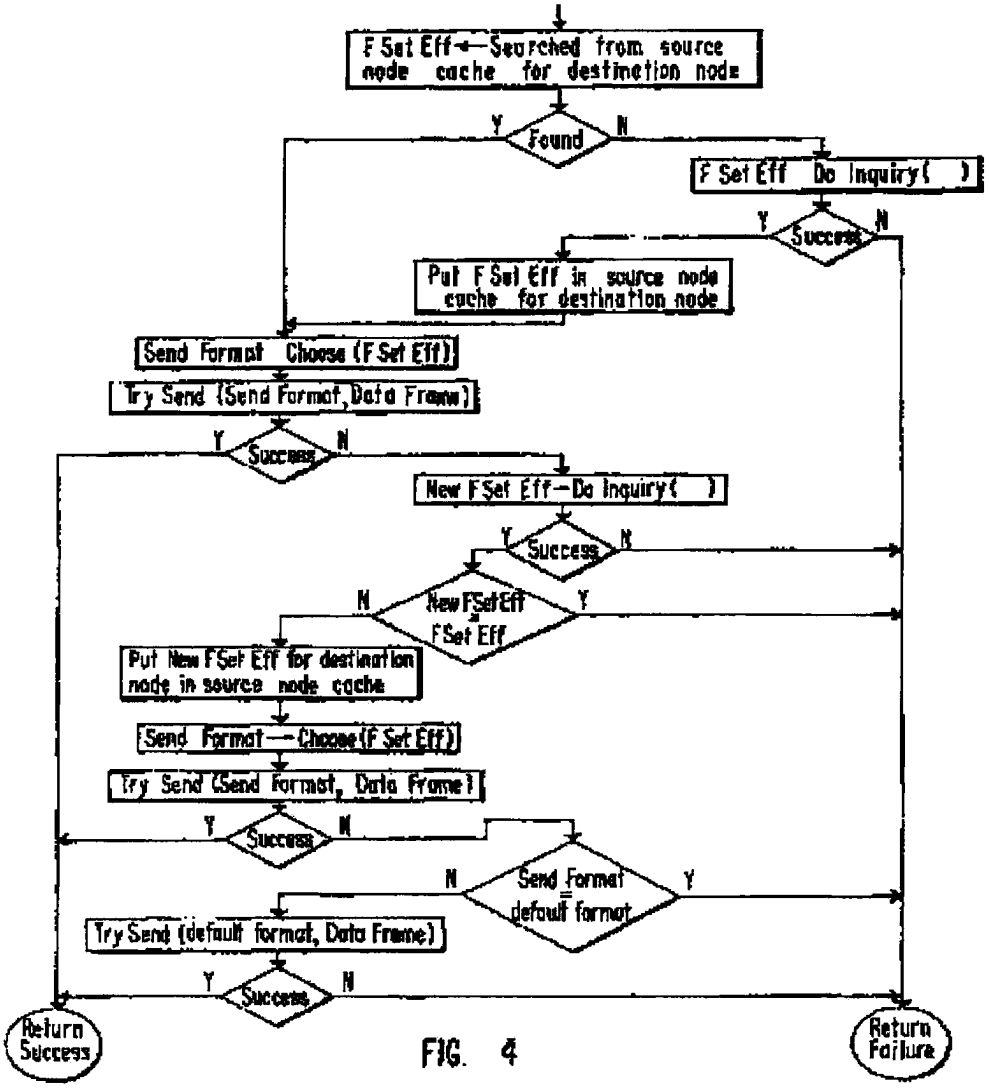

FIG. 4

*2 Intel asserted infringement of claims 1, 7, 15, and 18 of the '830 patent. Claims 1 and 7 are directed at networks (computer communications systems), while claims 15 and 18 are directed at chips.

Claim 1 of the '830 patent recites:

1. A computer communication system for transferring data between a plurality of nodes comprising:
(a) a communication medium;
(b) a plurality of nodes coupled to said communication medium for a transfer of data between said nodes; wherein said transfer of data is a transfer of data from a source node selected from said nodes to a destination node selected from said nodes, and
(c) transfer format selection means for selecting a format for the transfer of data from said source node to said destination node;
wherein said plurality of nodes is comprised of at least one default node and at least two supplemented nodes;

wherein each of said nodes has a format set comprised of one or more formats;
wherein said formats are defined in terms of data architecture;
wherein said data architecture is defined in terms of at least one member of a group consisting of encoding, encryption, compression, and protocol;
wherein each of said format sets includes at least one default format;
wherein said at least one default format is included in the format sets of each of said nodes;
wherein the format set of each of said supplemented nodes includes at least one supplemental format in addition to said at least one default format; and
wherein said transfer format selection means is adapted to select a format which is common to the format sets of the source node and destination node and which is compatible with said communication medium.
('830 patent, col. 11, lns. 23-55)

Claim 7 depends from claims 1, 2 and 6. Claims 2, 6 and 7 read:

2. A computer communication system in accordance with claim 1 wherein said transfer format selection means is comprised of a source node cache for node format sets and a destination node cache for node format sets; and wherein transfer format selection is made by the source node by searching for the destination node format set in said source node cache and by selecting a format which is included in said destination node format set and the source node format set.
6. A computer communication system in accordance with claim 2 wherein said format sets are represented by bit strings.
7. A computer communication system in accordance with claim 6 wherein bit positions of said bit strings represent formats.
('830 patent, col. 11, lns. 56-64; col. 12, lns. 22-24; col. 12, lns. 25- 27)

Claim 15 of the '830 patent recites:

15. A network interface for interfacing with a network having nodes and for supplementing the nodes of the network, said network interface comprising:
(a) at least one supplemental format, and
(b) transfer format selection means for selecting a format for the transfer of data from a source node to a destination node;
*3 wherein said network is comprised of a communication medium and a plurality of nodes coupled to said communication medium for the transfer of data between nodes;
wherein said transfer of data is a transfer of data from a source node selected from said nodes to a destination node selected from said nodes;
wherein each of said nodes has a format set comprised of at least one default format common to each format set;
wherein said network interface is adapted to supplement a node selected from said nodes by adding said at least one supplemental format to the format set of said selected node;
wherein said transfer selection means is adapted to select a format which is common to the format sets of the source node and destination node and which is compatible with said communication medium; and
wherein said formats are defined in terms of data architecture; wherein said data architecture is defined in terms of at least one member of the group consisting of encoding, encryption, compression and protocol.
('830 patent, col. 12, ln. 62--col. 13, ln. 24)

Claim 18 depends from claims 15, 16 and 17. Claims 16, 17 and 18 read:

16. A network interface in accordance with claim 15 wherein said transfer format selection means is comprised of a source node cache for node format sets; and wherein transfer format selection is made by the source node by searching for the destination node format set in said source node cache and by selecting a format which is included in said destination node format set and the source node format set.
17. A network interface in accordance with claim 16 wherein said format sets are represented by bit strings.
18. A network interface in accordance with claim 17 wherein bit positions of said bit strings represent formats.
('830 patent, col. 13, lns. 25-32; col. 13, lns. 33-34; col. 13, lns. 35- 37)

The court construed the disputed terms of the asserted claims of the '830 patent. The most significant constructions for the purposes of resolving the parties' post-trial motions are as follows: [FN1]

FN1. The recited claim construction was provided to the jury in the final jury instructions. The court's complete claim construction opinion for the '830 patent is provided in *Intel Corp. v. Broadcom Corp.*, 172 F.Supp.2d 478 (D.Del.2001).

(1) "A plurality of nodes coupled to said communication medium for a transfer of data between said nodes; wherein said transfer of data is a transfer of data from a source node selected from said nodes to a destination node selected from said nodes."

The term "node" means any data processing device, including, but not limited to, a computer, a file server, a bridge, a gateway, a co-processor, modem server, memory, or printer, that includes a network interface, through which it is coupled to the communication medium. While a node must be a device that includes a network interface, it does not as part of its own definition have to be coupled, or electronically connected, to the communication medium. Source nodes and destination nodes are not limited to the original source of the data to be transmitted or the ultimate destination of the transmitted data.

The term "transfer" means "to transmit something from one node to another." The term "data" means anything passed between nodes that conveys meaning. The term "source node" means "node" as defined above, that has the capability to transmit data. A "destination node" is a "node," as defined above, that has the capability of receiving data.

*4 (2) "Transfer format selection means for selecting a format for the transfer of data from said source node to said destination node ... wherein said transfer format selection means is adapted to select a format which is common to the format sets of the source node and destination node and which is compatible with said communication medium."

The term "data" means anything passed between nodes that conveys meaning. This claim element is in means-plus-function format. The claimed function is selecting a format for the transfer of data from said source node to said destination node, which is common to the format sets of the source node and the destination node and which is compatible with said communication medium.

The corresponding structure is (1) a bit string representation of the destination node's supported format set; (2) that is retrieved in accordance with an algorithm disclosed in Figure 4 that first searches the source node's associated memory, and then, if necessary, conducts an inquiry dialog; and (3) any circuitry configuration or any software programmed to execute an algorithm that first uses the bit string representation of the destination node's supported format set to determine which transfer formats are common to the transfer format sets of the source node and the destination node and compatible with the communication medium and then selects one transfer format from those common transfer formats to use in transmitting the information to the destination node.

The term "source node" is a "node" as defined above, that has the capability to transmit data. A "destination node" is a "node," as defined above, that has the capability of receiving data. The source node does not have to be the original source of data being transmitted. The "selected from said nodes" phrase that modifies both the source node and the destination node simply requires the source node and the destination node to each be one of the plurality of nodes that is referenced earlier in the claim.

(3) "Wherein said plurality of nodes is comprised of at least one default node and at least two supplemented nodes."

The term "plurality" standing alone, means at least two. However, the plurality of nodes referred to in the claims is limited by the wherein clause that describes that the plurality must be "comprised of" at least one default node and at least two supplemented nodes. Therefore, as used in claim 1, the term "plurality" requires at least three nodes. The term default node is a node coupled to the communication medium which can transfer data over the network only in the default format or default formats. The term supplemented node is a node coupled to the communication medium which can transfer data over the network in the default format or default formats and which can also transfer data over the network in one or more supplemental formats.

(4) "Wherein each of said format sets includes at least one default format wherein said at least one default format is included in the format sets of each of said nodes."

***5** The term default format means a common format that every node coupled to the communication medium can use to transfer data to every other node coupled to that medium.

(5) "Wherein the format set of each of said supplemented nodes includes at least one supplemental format in addition to said at least one default format."

The term supplemental format means an additional format, distinct from the default format, that is not common to all nodes coupled to the network.

(D.I. 689 at 25-28)

2. The '201 Patent

The '201 patent, the '630 patent, and '478 patents (collectively "the digital video patents") generally relate to devices that implement techniques used to reduce digital data volume and then expanding the

data back to its original state so that it can be displayed and viewed normally. These techniques are commonly referred to as compression or encoding and decompression or decoding. All of these patents relate to compression or decompression of digital video data.

Specifically, the invention of the '201 patent is a singlechip integrated circuit that enables the decompression of compressed full motion video data in real time. The claimed video processor includes a statistical decoder, a pixel interpolator, and arithmetic logic circuitry, all of which are controlled by a sequencer.

The statistical decoder decompresses information that has been compressed using statistical encoding. Statistical encoding is an encoding technique that involves assigning short bit strings for data that occurs frequently, and long codes for data that occurs infrequently.

The pixel interpolator of the '201 patent is used in the decoding of inter-frame coded images. Inter-frame coding refers to a coding technique that uses differences between an initial frame and a subsequent frame to encode and compress the frame data (i.e., instead of sending the full subsequent frame, the decoder sends the differences between the initial frame and the subsequent frame and the decoder than reconstructs the subsequent frame using this information). Operating on the pixels from the previously decoded image, the pixel interpolator generates "interpolated pixel values" that approximate pixel values between the pixel values from the previously decoded image retrieved from memory.

The arithmetic logic circuitry performs arithmetic operations (such as addition) or logical operations (such as AND or OR). For example, during inter-frame encoding, arithmetic logic circuitry may be used to add interpolated pixel values from the previously decoded video image to error data from the current video image.

The sequencer conditions the statistical decoder, pixel interpolator, and arithmetic logic circuitry to operate simultaneously to produce decompressed pixel data. As compared with each element performing its function in serial, simultaneous operation allows the decoding process to be performed faster.

Intel asserts infringement of claims 1 and 10 of the '201 patent.

***6** Claim 1 is directed to a video signal processor. The video signal processor includes an input means, a statistical decoding means, a pixel interpolating means, an arithmetic data processing means, an output means, and a sequencing means. Specifically, claim 1 of the '201 patent recites:

> 1. A video signal processor including:
> input means for applying digital data representing a video image including compressed video data and pixel data, wherein a portion of said digital data is statistically encoded;
> statistical decoding means, coupled to said input means and responsive to a control signal for decoding the statistically encoded digital data provided by said input means to generate decoded digital data;
> pixel interpolating means, responsive to said control signal and to the pixel data provided by said input means for developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data;
> arithmetic data processing means, responsive to said control signal, for performing arithmetic operations on the digital data provided by said statistical decoding means and on the interpolated pixel values provided by said pixel interpolating means;
> output means, coupled to said arithmetic data output means, processing means for providing processed video data from said arithmetic data processing means as an output signal; and
> sequencing means for generating said control signal to condition said statistical decoding means, said arithmetic data processing means and said pixel interpolating means to operate simultaneously to produce decoded and decompressed pixel data as said output signal.
> ('201 patent, col. 60, lns. 4-35)

Claim 10 is directed to an integrated circuit for processing compressed video signals to provide decompressed video signals. The claimed integrated circuit includes an I/O port, an address output port, a statistical decoder, I/O circuitry, a pixel interpolator, an arithmetic processing means, a selectively interconnecting means, a control means, and an address generating means. Specifically, claim 10 of the '201 patent recites:

> 10. An integrated circuit for processing compressed video signal, segments of which having been encoded using different encoding processes, to provide decompressed video signal representing

moving images, said integrated circuit comprising:
an I/O port for coupling said integrated circuit to memory means;
an address output port for coupling address signals to said memory means;
a statistical decoder coupled to said I/O port for decoding variable-length-encoded compressed video signals;
I/O circuitry coupled to said I/O port, for providing processed video signal to said I/O port, and for accepting a processed video signal from said I/O port;
a pixel interpolator for generating values representing pixels interstitial to pixel values represented by said processed video signal;
*7 arithmetic processing means responsive to control signals, for performing arithmetic and Boolean functions on binary values;
means responsive to further control signals for selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator and said arithmetic processing means;
control means for generating said control signals and said further control signals to selectively condition said arithmetic processing means to perform one of a plurality of decoding algorithms on compressed video data provided at said I/O port; and
address generating means coupled to said address output port and responsive to at least said control means for generating memory address signals for said memory means.
('201 patent, col. 61, ln. 45--col. 62, ln. 32)

The court construed the disputed terms of the asserted claims of the '201 patent. The most significant constructions for the purposes of resolving the parties' post-trial motions are as follows: [FN2]

> FN2. The recited claim construction was provided to the jury in the final jury instructions. The court's complete claim construction opinion for the '201 patent is provided in *Intel Corp. v. Broadcom Corp.*, 172 F.Supp.2d 515 (D.Del.2001).

(1) "Statistical decoding means, coupled to said input means and responsive to a control signal for decoding the statistically encoded digital data provided by said input means to generate decoded digital data."
This claim element is in a means-plus-function format. The function is decoding the statistically encoded digital data provided by said input means to generate decoded digital data.
The term "control signal" means an electronic signal used to control internal or external devices or processes.
The statistical decoder must be responsive to the same control signal that is generated by the sequencing means to condition the statistical decoding means, the arithmetic processing means and the pixel interpolating means of claim 1. The term "responsive" means to respond or react.
The corresponding structure is the statistical decoding circuitry 1014, and structural equivalents.
The term "coupled" means electrically connected directly or indirectly.
(2) "Pixel interpolating means, responsive to said control signal and to the pixel data provided by said input means for developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data."
This claim element is in means-plus-function format. The function, as recited in the claim, is "developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by pixel data." The function means that pixel values are created for a current image being decoded that are between pixels from a previously decoded image.
The pixel values are created for a current image being decoded that are between pixels from a previously decoded image. The term "pixel data" refers to decoded pixel data from a previously decoded image.
The pixel interpolating means must be responsive to the same control signal that is generated by the sequencing means to condition the statistical decoding means, the arithmetic processing means and the pixel interpolating means of claim 1. As stated above, the term "responsive" means to respond or to react.
*8 The corresponding structure is subtractor 824, multiplier 825, adders 856 and 858, and two input registers, and structural equivalents.
(3) "Arithmetic data processing means, responsive to said control signal, for performing arithmetic operations on the digital data provided by said statistical decoding means and on the interpolated pixel values provided by said pixel interpolating means."
This element is written in means-plus-function format. The function of the "arithmetic data processing means" is to perform arithmetic operations (e.g., addition, subtraction, multiplication, and/or division) on digital data provided by the "statistical decoding means" and

on the interpolated pixel values provided by the "pixel interpolating means."

The arithmetic data processing means [is] to be responsive to the control signal that is generated by the sequencing means to condition the statistical decoding means, the arithmetic processing means and the pixel interpolating means of claim 1. As stated above, the term "responsive" means to respond or react.

The corresponding structure for the "arithmetic data processing means" is adder 450 or adder 452, and structural equivalents. Performing "arithmetic operations" does not require the performance of both addition and subtraction. For example, a structure that performs only successive addition operations satisfies the function of performing arithmetic operations.

(4) "Sequencing means for generating said control signal to condition said statistical decoding means, said arithmetic data processing means and said pixel interpolating means to operate simultaneously to produce decoded and decompressed pixel data as said output signal."

This claim element is in means-plus-function format. The "sequencing means" performs the function of generating a control signal to condition the operation of the "statistical decoding means," the "arithmetic data processing means" and the "pixel interpolating means" to operate simultaneously.

The above components--the statistical decoding means, the arithmetic data processing means, and the pixel interpolating means--are required by the claim language to be responsive to (i.e., each component must be able to respond or react to) this control signal such that when the control signal is received, the component is put into a specified state.

The corresponding structure of the sequencing means is the microcode RAM 310, instruction register 316, multiplexor 320, and a portion of the control block 308 that generates the LI and MXC signals, and structural equivalents. The term "to condition" means to put into a specified state.

(5) "Arithmetic processing means responsive to control signals, for performing arithmetic and Boolean functions on binary values."

This claim element is in means-plus-function format. The arithmetic processing means performs arithmetic and Boolean functions on binary values. "Arithmetic functions" are one or more of the operations of addition, subtraction, division, or multiplication. "Boolean functions" are one or more of the logical operations that can be performed on binary data such as AND, OR, NOT or XOR. "Binary values" are data represented by 1s and 0s.

***9** [T]he function of this claim element is "performing arithmetic and Boolean functions on binary values." Thus, the function of the "arithmetic processing means" is to perform operations which include both arithmetic functions (e.g., addition or subtraction) and Boolean functions (e.g., AND or NOT) on data values represented by 1s and 0s.

The corresponding structure of arithmetic processing means of claim 10 is the corresponding structure of the claim 1 arithmetic processing means and one or more of the Boolean logic gates (such as OR, NOR, XOR, AND, or NOT) depicted in Figure 4B, and structural equivalents. A structure that performs only successive addition operations satisfies the function of performing arithmetic operations.

(6) "Means responsive to further control signals for selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator and said arithmetic processing means."

This claim element is in means-plus-function format. The function, as recited in the claim, is "selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator and said arithmetic processing means." The recited function is to connect the four stated elements to each other and not merely to connect those four elements to other elements on the chip.

The corresponding structure of the means responsive to further control signals is either 1) any one of the general purpose registers of the register file 510; 2) the bus gate 520; or 3) the input registers contained in the statistical decoder, pixel interpolator, and ALU, and structural equivalents.

(7) "Control means for generating said control signals and said further control signals to selectively condition said arithmetic processing means to perform one of a plurality of decoding algorithms on compressed video data provided at said I/O port."

This claim element is in means-plus-function format. The function of the "control means" is to generate control signals to selectively condition the arithmetic processing means to perform one of a plurality of decoding algorithm on video data.

The term "control signal" means an electronic signal used to control internal or external devices or processes. The term "condition" means "to put into a specified state." The control signal contains instructions that are read by the arithmetic processing means. The arithmetic processing means responds to these instructions by performing

the specified type of decoding called for in the control signal.
The corresponding structure of the control means is the microcode RAM 310, instruction register 316, multiplexor 320, and a portion of the control block 308 that generates the LI and MXC signals, and structural equivalents.
(D.I.689)

C. The Accused Products

Intel alleged that Broadcom's Ethernet compliant "PHY chips," which implement a feature called auto-negotiation to automatically configure the transmission protocols and formats used by new devices added to a network, infringe the asserted claims of its '830 patent. PHY chips (of which Broadcom's BCM 5228 and 5040 products are representative) are attached to devices, such as computers or printers, so that the devices can be connected to a computer network. Broadcom's PHY chips are designed to be used in an Ethernet network.

***10** In addition, Intel alleged that Broadcom's digital video decoding devices (of which Broadcom's BCM 7010 and 7020 products are representative) infringe the asserted claims of its '201 patent.

D. Procedural History [FN3]

> FN3. On September 6, 2000, this action was assigned to the Honorable Roderick R. McKelvie. Judge McKelvie ruled on the pretrial motions and issued the claim construction opinions. He also presided over the trial. On January 23, 2002 this action was reassigned to Chief Judge Sue L. Robinson. Judge McKelvie resigned from the office of United States District Judge on June 28, 2002.

On October 10, 2000, defendant moved to dismiss plaintiff's complaint or, in the alternative, to transfer the action to the United States District Court for the Northern District of California. After eleven months of discovery, the court heard oral argument on defendant's motion on September 24, 2001. In a memorandum opinion dated October 9, 2001, the court denied defendant's motion. Defendant subsequently answered plaintiff's complaint on October 23, 2001. As defendant had indicated it would in earlier interrogatory responses, the answer included a number of affirmative defenses relating to license agreements.

In anticipation of these affirmative defenses, plaintiff filed three sets of partial summary judgment motions relating to defendant's license defenses. The first concerned a January 22, 1995 Intel Product Development and License Agreement (the "Joint Development Agreement") between plaintiff and defendant. Plaintiff moved for summary judgment that defendant's allegedly infringing products are not licensed under the '830 or '410 patents, arguing that the scope of the Joint Development Agreement does not include a license for defendant to make, sell, or use the accused products in this suit under either the '830 or '410 patent. The second and third motions concern the effect of licenses between plaintiff and numerous third parties to whom defendant sells its allegedly infringing products (the "Intel licensees"). Defendant contends that the licenses, which give the Intel licensees the right to "have [the products] made," insulates defendant to the extent it sells the allegedly infringing products to the Intel licensees. Plaintiff contends that these licenses do not insulate defendant's infringement as a matter of law. Defendant cross-moved for summary judgment on these two motions, contending that it is licensed as a matter of law.

On September 24, 2001, the court heard oral argument in accordance with *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996), to construe the claims of the patents.

In order to simplify the issues before the jury and to shorten the length of the jury trial, the court required that the trial proceed in two parts. The first trial was to be a three-week jury trial on the '830 and '201 patents. A subsequent trial would cover the remaining patents.

On November 6, 2001, the court issued two claim construction opinions regarding the '830 and '201 patents. *See Intel Corp. v. Broadcom Corp.*, 172 F.Supp.2d 478 (D.Del.2001); *Intel Corp. v. Broadcom Corp.*, 172 F.Supp.2d 515 (D.Del.2001).

On November 20, 2001, the court issued a memorandum opinion addressing the motions regarding defendant's license defense. *See Intel Corp. v. Broadcom Corp.*, 173 F.Supp.2d 201 (D.Del.2001). Therein, the court granted plaintiff's motions for partial summary judgment that the Joint Development Agreement does not include a license on the '830 or '410 patents, and that the Motorola license agreement does not confer a license to defendant for products sold to Motorola subsidiary,

General Instrument. As to the remainder of the licenses containing "have made" rights, the court reasoned that "[a]n unlicensed third party in the position of Broadcom only is afforded the protections of [such] a license if those protections are conveyed by the licensee to the third party as an exercise of the licensed party's 'have made' rights." *Intel*, 173 F.Supp.2d at 203. The court found

> ***11** that genuine issues of material fact remain as to whether the sale transactions to Intel licensees conveyed any of those licensees' rights to Broadcom. Accordingly, the court will deny both parties' summary judgment motions. Should Broadcom be unable, at trial or through documents submitted with post-trial briefing, to set forth any such facts, this license defense will be without legal merit. However, should Broadcom set forth facts that indicate that Broadcom was indeed making these allegedly infringing products in response to requests by Intel licensees 'to make' them, Broadcom may pursue this defense.

Id. at 235. The court also found that the licenses did not cover the '830 or '410 patents.

E. The Trial

The parties tried their claims regarding the '830 and '201 patents to a jury from November 28, 2001 to December 14, 2001. The jury returned a verdict finding that: (1) the accused products did not infringe any of the asserted claims of the '830 or '201 patents; (2) the asserted claims of the '830 patent were each invalid as anticipated by and as obvious in view of the Flashtalk/Flashcard prior art product; (3) defendant owes no damages to plaintiff; and (4) defendant had authority to sell products accused of infringing plaintiff's '201 and '830 patents to twelve of plaintiff's third-party licensees by virtue of those licensees' agreements with plaintiff.

The verdict form required the jury to mark which limitations they found were absent from the accused products that they found not to infringe. The jury found the following limitations missing:

'830 patent, claim 1:(1) transfer format selections means for selecting a format for the transfer of data from said source node to said destination node ("TFSM" or "transfer format selection means"); (2) wherein each of said format sets includes at least one default format; and (3) wherein said transfer format selection means is adapted to select a format which is common to the format sets of the source node and destination node and which is compatible with said communication medium.

'830 patent, claim 7:(1) a computer communication system in accordance with claim 1; (2) wherein said transfer format selection means is comprised of a source node cache for source node format sets and a destination node cache for node format sets; and (3) wherein transfer format selection is made by the source node by searching for the destination node format set in said source node cache and by selecting a format which is included in said destination node format set and the source node format set.

'830 patent, claim 15:(1) at least one supplemental format; (2) transfer format selection means for selecting a format for the transfer of data from a source node to a destination node; (3) wherein each of said nodes has a format set comprised of at least one default format common to each format set; (4) wherein said network interface is adapted to supplement a node from said nodes by adding said at least one supplemental format to the format set of said selected node; and (5) wherein said transfer format selection means is adapted to select a format which is common to the format sets of the source node and destination node and which is compatible with said communication medium.

***12** '830 patent, claim 17:(1) a network interface in accordance with claim 15; (2) wherein said transfer format selection means is comprised of a source node cache for node format sets; and (3) wherein transfer format selection is made by the source node by the source node by searching for the destination node format set in said source node cache and by selecting a format which is included in said destination node format set and the source node format set.

'201 patent, claim 1:(1) pixel interpolating means, responsive to said control signal and to the pixel data provided by said input means for developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data ("pixel interpolating means"); (2) arithmetic data processing means, responsive to said control signal for performing arithmetic operations on the digital data provided by said statistical decoding means and on the interpolated pixel values provided by said pixel interpolating means ("arithmetic data processing means"); and (3) sequencing means for generating said control signal to condition said statistical decoding means, said arithmetic processing means, and said pixel interpolating means to operate simultaneously to produce decoded and decompressed pixel data as said output signal ("sequencing means").

'201 patent, claim 10:(1) arithmetic processing means responsive to control signals, for performing

arithmetic and Boolean functions on binary values ("arithmetic processing means"); (2) means responsive to further control signals for selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator, and said arithmetic processing means ("means responsive").

III. STANDARDS OF REVIEW

A. Motion for Judgment as a Matter of Law

To prevail on a renewed motion for judgment as a matter of law following a jury trial, the moving party " 'must show that the jury's findings, presumed or express, are not supported by substantial evidence or, if they were, that the legal conclusions implied [by] the jury's verdict cannot in law be supported by those findings." ' *Pannu v. Iolab Corp.*, 155 F.3d 1344, 1348 (Fed.Cir.1998) (quoting *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 893 (Fed.Cir.1984)). " 'Substantial' evidence is such relevant evidence from the record taken as a whole as might be acceptable by a reasonable mind as adequate to support the finding under review." *Perkin-Elmer Corp.*, 732 F.2d at 893. In assessing the sufficiency of the evidence, the court must give the non-moving party, "as [the] verdict winner, the benefit of all logical inferences that could be drawn from the evidence presented, resolve all conflicts in the evidence in his favor, and in general, view the record in the light most favorable to him." *Williamson v.. Consol., Rail Corp.*, 926 F.2d 1344, 1348 (3d Cir.1991); *Perkin-Elmer Corp.*, 732 F.2d at 893. The court may not determine the credibility of the witnesses nor "substitute its choice for that of the jury between conflicting elements of the evidence." *Perkin-Elmer Corp.*, 732 F.2d at 893. In sum, the court must determine whether the evidence reasonably supports the jury's verdict. *See Dawn Equip. Co. v. Ky. Farms Inc.*, 140 F.3d 1009, 1014 (Fed.Cir.1998).

B. Motion for a New Trial

***13** Federal Rule of Civil Procedure 59(a) provides, in pertinent part:

> A new trial may be granted to all or any of the parties and on all or part of the issues in an action in which there has been a trial by jury, for any of the reasons for which new trials have heretofore been granted in actions at law in the courts of the United States.

Fed.R.Civ.P. 59(a). The decision to grant or deny a new trial is within the sound discretion of the trial court and, unlike the standard for determining judgment as a matter of law, the court need not view the evidence in the light most favorable to the verdict winner. *See Allied Chem., Corp. v. Darflon, Inc.*, 449 U.S. 33, 36, 101 S.Ct. 188, 66 L.Ed.2d 193 (1980); *Olefins Trading, Inc. v. Han Yang Chem. Corp.*, 9 F.3d 282 (3d Cir.1993); *LifeScan Inc. v. Home Diagnostics, Inc.*, 103 F.Supp.2d 345, 350 (D.Del.2000), *aff'd per curiam*, Nos. 00-1485, 00-1486, 2001 WL 345439 (Fed.Cir. Apr.6, 2001) (citations omitted). Among the most common reasons for granting a new trial are: (1) the jury's verdict is against the clear weight of the evidence, and a new trial must be granted to prevent a miscarriage of justice; (2) newly-discovered evidence exists that would likely alter the outcome of the trial; (3) improper conduct by an attorney or the court unfairly influenced the verdict; or (4) the jury's verdict was facially inconsistent. *See Zarow-Smith v. N.J. Transit Rail Operations*, 953 F.Supp. 581, 584 (D.N.J.1997) (citations omitted). The court must proceed cautiously, mindful that it must not substitute its own judgment of the facts and the credibility of the witnesses for those of the jury. The court should grant a new trial on the basis that the verdict was against the weight of the evidence only where a miscarriage of justice would result if the verdict were to stand. *See Williamson*, 926 F.2d at 1352; *EEOC v. Del. Dep't of Health and Soc. Servs.*, 865 F.2d 1408, 1413 (3d Cir.1989).

IV. INTEL'S MOTION FOR JUDGMENT AS A MATTER OF LAW FOR INFRINGEMENT, VALIDITY, AND DAMAGES OF THE '830 PATENT

A. Infringement

A determination of infringement requires a two-step analysis. First, the court must construe the asserted claims so as to ascertain their meaning and scope. Second, the claims as construed are compared to the accused product. *See KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1355 (Fed.Cir.2000). Claim construction is a question of law while infringement is a question of fact. *See id.* To establish literal infringement, "every limitation set forth in a claim must be found in an accused product, exactly." *Southwall Tech., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1575 (Fed.Cir.1995). An accused product that does not literally infringe a claim may still infringe under the doctrine of equivalents if each limitation of the claim is met in the accused product either literally or equivalently. *See Sextant Avionique, S.A. v. Analog Devices, Inc.*, 172 F.3d 817, 826 (Fed.Cir.1999).

***14** The jury concluded that Broadcom's accused products did not infringe claims 1, 7, 15, and 18 of the '830 patent.

In its motion for judgment as a matter of law for infringement of the '830 patent, Intel contends that it fully met its burden of proving, by a preponderance of the evidence, that Broadcom's internal network infringes every claim limitation of claims 1 and 7 of the '830 patent and that Broadcom's accused BCM 5228 and 5040 products infringe every claim limitation of claims 15 and 18 of the '830 patent. Intel notes that while its experts Drs. Scholl and Rhyne provided detailed testimony as to how the accused products and network meet every limitation of the asserted claims of the '830 patent, Broadcom did not call its expert to testify that any of the limitations of any of the four asserted claims were missing from the accused products or network. Instead, Broadcom's "sole attempt to lay out a non-infringement case was through its cross-examination of Intel's experts ... based on improper claim construction ... and irrelevant additional features of the accused products that are outside the scope of the claims--none of which diminished Intel's proof of infringement." (D.I. 725 at 1-2)

In reply, Broadcom correctly states that the only question raised by Intel's motion is whether "viewing the evidence in the light most favorable to [Broadcom] and giving [Broadcom] the advantage of every fair and reasonable inference, there is insufficient evidence from which a jury could reasonably find [non-infringement.]" [FN4] *Wittekamp v. Gulf & Western Inc.*, 991 F.2d 1137, 1141 (3rd Cir.1993). Furthermore, the source of evidence that supports the jury's verdict (e.g., cross-examination of Intel's experts, documents, or fact witnesses) is legally irrelevant to accessing the sufficiency of the evidence. *See Mas-Hamilton v. LaGard, Inc.*, 156 F.3d 1206, 1215 (Fed.Cir.1998). Broadcom contends that the evidence presented was sufficient to establish that the accused products do not infringe.

> FN4. The court notes that Intel has consistently failed to argue the appropriate standard of review in the numerous post-trial briefs filed in the case at bar. Intel argues why sufficient evidence exists for the jury to find in its favor. The court emphasizes that the appropriate standard for review of a jury verdict on a motion for judgment as a matter of law is the moving party " 'must show that the jury's findings, presumed or express, are not supported by substantial evidence[.]" ' *Pannu v. Iolab Corp.*, 155 F.3d 1344, 1348 (Fed.Cir.1998) (quoting *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 893 (Fed.Cir.1984)).

Proving infringement was Intel's burden. *Novartis Corp. v. Ben Venue Laboratories, Inc.*, 271 F.3d 1043, 1046 (Fed.Cir.2001). Thus, Broadcom's failure to put on its own expert to testify as to non-infringement is not fatal to its case. Broadcom was not required to put on its own expert to disprove infringement because it was Intel that bore the burden of proving infringement. Broadcom built its non-infringement case from cross-examining Intel's experts. Broadcom also impeached the credibility and impartiality of Intel's main expert, Dr. Rhyne, who may have appeared to the jury like he was a "professional witness" with financial interest in Intel and a long-standing and lucrative relationship with Intel's counsel. (D.I. 708 at 2829-2835)

The sole task for the court is to determine whether there is sufficient evidence in the record from which a reasonable jury could conclude that Broadcom does not infringe the asserted claims. Here, it makes most sense to analyze the limitations within the claim elements that the jury concluded were not present in the accused products.

1. Transfer format selection means

a. TFSM Function

***15** The court construed "source node" to be "a node that has the capability to transmit data," and construed "destination node" to be "a node that has the capability to receive data."

The court rejected Broadcom's construction that the terms "source node" and "destination node" should be construed to mean the device that initiates the transfer of data and the device that is the intended final recipient of the data, respectively. Broadcom had advanced this argument so that "switched" Ethernet networks, as depicted in Exhibit 2509, would fall outside the claims (because all data travels through an intermediate point--the switch). Exhibit 2509 shows two computers (one can transmit at 10 Mbps or 100 Mbps and one at 10 Mbps only), each linked to a switch (that can transmit at 10 Mbps or 100 Mbps) that sits between them. All data flow between the two computers travels through the switch.

Under the court's construction, the switch acts as a destination node when it receives data from the first node and acts as a source node when it sends data to the second node.

Broadcom, using Exhibit 2509 to cross-examine Dr. Rhyne, asked him whether the two computers on either side of the switch auto-negotiate with each other. He stated that they did not. Broadcom contends that this shows that the function of the TFSM, "selecting a format for the transfer of data from said source node to said destination node ... that is common to both of them," is not met.

This argument is without merit. Under the court's claim construction, it does not matter that the two computers do not auto-negotiate directly with each other--both auto-negotiate (i.e., perform the function of selecting a common format for the transfer of data) with the intermediate node (the switch). Under the court's claim construction, the switch, which contains PHY chips just like those in the computers, is a source node and a destination node. Thus, the court finds that no reasonable juror could conclude that the function of the TFSM is not present in the accused products.

b. TFSM Structure

According to the claim construction, part (2) of the structure retrieves a bit string representative of the format set "in accordance with an algorithm disclosed in Figure 4 that first searches the source node's associated memory, and then, if necessary, conducts an inquiry dialog[.]" *Intel*, 172 F.Supp.2d at 506.

Broadcom relies upon the cross-examination of Dr. Rhyne in arguing that the first thing that always happens when auto-negotiation is performed is the accused PHY chips transmit and receive signals called FLP's. Broadcom also cites the testimony of Mr. Gary Huff that the accused PHY chips do not ever attempt to retrieve information about the format supported by any other machine by first searching any memory or anything else before sending out FLP's. "It always just sends out FLP's." (D.I. 706 at 2236) Broadcom argues that this evidence proves that the TFSM structure is not present in the PHY chips, because claim construction requires the TFSM to first search its memory before performing the inquiry dialog.

***16** Intel alleges that the FLP's are the "inquiry dialog" referred to in step 2 of the TFSM structure. Intel contends that the answers of Dr. Rhyne and the testimony of Mr. Huff do not prove anything relevant. It argues that Dr. Rhyne clarified that the FLP's come out first when it is powered up, because at that point the PHY chip does not know any other format sets, so it does not need to check its memory. There is a single bit (set to 0 initially) that indicates whether an inquiry dialog is necessary or not. This bit is checked first--corresponding to the first search--and if necessary (when the bit is set to 0), it conducts an inquiry dialog.

In response, Broadcom contends that Dr. Rhyne's testimony that the PHY chips first check the single bit before sending out FLP's contradicts his testimony on cross that the first thing that always happens is the PHY chips send out FLP's. In addition, it argues that determining whether a single bit has been checked is not retrieval from memory of a "bit string" as required by the court's claim construction. Moreover, Mr. Huff testified that the single bit is never checked by the Broadcom PHY itself (it is checked by an external device that controls the PHY).

The testimony about the FLP's provides substantial evidence for a reasonable jury to find that the structure of the TFSM is not contained in the accused devices. Thus, the court finds that Broadcom presented substantial evidence at trial to support the jury's conclusion that the claim elements that reference the TFSM are not present in the accused products.

2. "Default node/format" and "Supplemental node/format"

The term default format means "a common format that every node coupled to the communication medium can use to transfer data to every other node coupled to that medium." The term default node is "a node coupled to the communication medium which can transfer data over the network only in the default format or default formats."

The term supplemental format means "an additional format, distinct from the default format, that is not common to all nodes coupled to the network." The term supplemented node is "a node coupled to the communication medium which can transfer data over the network in the default format or default formats and which can also transfer data over the network in one or more supplemental formats."

Broadcom again relies on Exhibit 2509 and the cross-examination of Dr. Rhyne to support its

argument that the accused Ethernet networks do not have a "default node/format" or "supplemented node/format." Dr. Rhyne testified that when autonegotiation is performed the computer on the left will select 100 Mbps and the computer on the right will select 10 Mbps. As these are not common, Broadcom contends no default format exists. Since no default format exists, it follows that no supplemental format can exist.

This argument is without merit. As Intel points out, Broadcom analyzes the network only after the different pairs of nodes have negotiated to the optimum format for transfer of data. It is unsurprising that after doing so, some nodes determine that they speak only the default format (10 Mbps), while others will determine they speak a faster format (100 Mbps), and will thus use it. That is the whole point of the invention. The Broadcom chips "can use" (i.e., are capable of using) the default format 10 Mbps to transfer data--thus they have a default format. The fact that the chips do not use that format after auto-negotiating and picking a more optimal format to use is irrelevant. The same argument follows for "supplemental format," "supplemental node" and "adapted to supplement a node" claim limitations. Thus, the court finds that no reasonable juror could find that the accused products do not meet the "default node," "default format," "supplemental node" and "supplemental format" claim limitations.

3. "Source node cache" and "Destination node cache."

***17** The dispute regarding this claim limitation is solely one of claim construction. Claim construction is an issue of law for the court. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). This limitation was not disputed prior to trial, thus, the terms were not construed in the previous claim construction opinions.

Broadcom contends that claims 2 and 16 require "source node cache for node format sets," meaning that the source node cache must store more than one destination node format set. Intel responds by asserting that the term "sets" is plural because the source node cache stores both the source node format set and the destination node format set.

Having reviewed the patent specification and the relevant claims, the court holds that the claims only require more than one "format set," not more than one destination format set. Thus, a source node cache that stores both the source node format set and the destination node format set meets this claim limitation. Based on the evidence presented at trial, no reasonable jury could conclude that the accused products do not contain the "source node cache" and "destination node cache" claim limitations.

In sum, the court finds substantial evidence was presented regarding the absence of the structure of the transfer format selection means claim limitation in the accused products. The jury's finding that the claim elements containing the TFSM limitation are not present in the accused products is supported by substantial evidence. [FN5] Thus, Intel's motion for judgement as a matter of law for infringement of the '830 patent is denied.

> FN5. Intel's proof of inducement and contributory infringement follows from its proof of direct infringement. The jury found no direct infringement and, thus, no indirect infringement. As the court concludes there is sufficient evidence to support the jury's finding of no direct infringement, the finding of no inducement and contributory infringement is supported as well.

B. Invalidity

The jury concluded that claims 1, 7, 15, and 18 of the '830 patent were anticipated and rendered obvious by the Flashtalk/Flashcard ("Flashtalk") prior art reference. Broadcom was unable to procure an actual Flashtalk product. The one remaining Flashtalk product Broadcom located belonged to the inventor, Mr. Michael Pflaumer, and he would not allow Broadcom to open it up or take it. At trial, Broadcom used a later issued patent, United States Patent No. 4,884,266 ("the '266 patent"), to describe how the product worked. Mr. Pflaumer explained that the product worked as explained in the '266 patent. Broadcom also relied on documents to show that the Flashtalk product did in fact exist, and was prior art to the '830 patent. The '266 patent itself was not prior art.

In this case, Broadcom did not present a separate "combining references" obviousness defense. Broadcom's obviousness defense, like its anticipation defense, was based solely on the Flashtalk reference.

Intel's motion for judgment as a matter of law raises two issues to resolve with respect to the validity of the '830 patent. First, was there legally sufficient evidence regarding the Flashtalk product itself? Second, was there substantial evidence that the

Flashtalk product contained every element of the '830 invention?

1. Was there legally sufficient evidence regarding the Flashtalk product?

***18** Intel first contends that Broadcom's invalidity defense fails as a matter of law because it rests on improper evidence, including a hearsay magazine article, a patent that is not prior art, and deposition testimony of Flashtalk's inventor, Michael Pflaumer. Intel contends that the testimony of Mr. Pflaumer must be corroborated. *See Price v. Symsek*, 988 F.2d 1187, 1194 (Fed.Cir.1993); *Finnigan Corp. v. ITC*, 180 F.3d 1354, 1370 (Fed.Cir.1999). [FN6]

> FN6. There is no dispute that the Flashtalk product is prior art or that it was publicly used more than one year before the '830 application was filed. (D.I. 793 at 12)

Broadcom disputes these assertions, submitting that the September 14, 1987 magazine article about the Flashtalk product was not hearsay because it was offered for a non-hearsay purpose. Moreover, Broadcom argues that the evidence that the '266 patent describes the Flashtalk product is amply corroborated by comparing the patent itself with the testimony of Mr. Pflaumer, a third party with no interest in this litigation. According to Broadcom, this is sufficient to satisfy a "rule of reason" test. *See Sandt Tech., Ltd. v. Resco Metal and Prods, Corp.*, 264 F.3d 1344, 1350 (Fed.Cir.2001). Broadcom also argues that Mr. Pflaumer's testimony was used to show that the Flashtalk product was publicly used and offered for sale more than a year before the '830 application was filed, and not to show that Mr. Pflaumer was the prior inventor. In any event, his testimony was corroborated by the magazine article, the testimony of his business partner, Mr. Goldhaber, and the '266 patent.

Corroboration of a witness' oral testimony is required to invalidate a patent under 35 U.S.C. § 102. *See Finnigan Corp. v. International Trade Comm'n*, 180 F.3d 1354, 1367 (Fed.Cir.1999). This requirement exists regardless of whether or not the witness is an interested party or an uninterested party. *See id.* at 1367-68. Corroboration has been required by the courts "because of doubt that testimonial evidence alone in the special context of proving patent invalidity can meet the clear and convincing evidence standard to invalidate a patent." *Id.* at 1368.

There is no evidence that the '266 patent embodied anything other than the Flashtalk product and Mr. Pflaumer so testified. The disclosures of the '266 patent correspond to the product Mr. Pflaumer described. Intel's expert, Dr. Rhyne, testified there was "no basis to dispute" that the '266 patent accurately describes the Flashtalk product. (D.I. 708 at 2797-98) Therefore, the court finds that Mr. Pflaumer's testimony was amply corroborated by the '266 patent.

2. Was there substantial evidence that the Flashtalk product contained every element of the '830 invention?

Intel contends that the Flashtalk product did not contain (1) the TFSM structure (as required by all asserted claims), or (2) "format sets ... represented by bit strings; wherein bit positions of said bit strings represent formats" (as required by claims 7 and 18).

At trial, Broadcom's expert, Dr. Tobagi, went through the claims element by element and explained his opinion as to why each element was present in the Flashtalk product.

a. TFSM Structure

***19** Intel argues that the Flashtalk product does not retrieve a bit string representation of the destination node's format from the destination node and that the Flashtalk product always sends an inquiry dialog as opposed to only if necessary--limitations in the second component of the structure of the court's claim construction of the TFSM limitation. *See Intel*, 172 F.Supp.2d at 506 ("[T]he corresponding structure ... of the transfer format selection means is: (1) a bit string representation of the destination node's supported format set; (2) that is retrieved in accordance with an algorithm disclosed in Figure 4 that first searches the source node's associated memory, and then, if necessary, conducts an inquiry dialog[.]").

Intel's argument attempts to add language to the court's claim construction. The claim construction does not require the transfer format selection means to retrieve a bit string representation of the destination node's format set from the destination node. Although the court's claim construction noted that "[i]n the embodiment described, ... the destination node sends back to the source node (using the default format) a bit string representation of its format set," *Intel*, 172 F.Supp.2d at 504, this was not a limitation as defined by the court's claim construction to the jury.

The Flashtalk product does not receive a bit string representation of the destination node's format set, but rather creates a bit string representation from the information received. This created bit string representation is then stored in memory by the Flashtalk product. The bit string representation is retrieved--as required by the court's claim construction--from the memory. The court finds that a reasonable jury could find the first part of the structure of the TFSM claim element present in the Flashtalk product.

Intel also argues that the Flashtalk product always sends an inquiry dialog instead of only if necessary as required by the claim construction. The Flashtalk product sends a "request to send" message to the destination node. Intel argues the "request to send" message is the "inquiry dialog" described in the claim construction and that this "request to send" dialog is always sent by the Flashtalk product.

Broadcom counters that the "request to send" is not an inquiry dialog and that Dr. Tobagi testified that the Flashtalk product performs an inquiry dialog only if necessary.

Dr. Tobagi's testimony provides substantial evidence regarding the operation of the Flashtalk product and its relation to the court's claim construction. The jury had substantial evidence to find that the inquiry dialog is performed only if necessary.

Under the court's claim construction, substantial evidence exists to support the jury's conclusion that the Flashtalk product meets the TFSM limitation.

b. Format Sets Represented by Bit Strings

Intel further argues that the Flashtalk product does not contain "format sets ... represented by bit strings; wherein bit positions of said bit strings represent formats" (as required by claims 7 and 18). Intel asserts that the bits used by the Flashtalk product do not represent a format and are not a bit string as required by the claims. Broadcom argues that the Flashtalk product stores two bits (representing a high-speed frame and a low-speed frame) and that each of these bits represents a separate format and together form a bit string.

*20 The jury was presented with contradictory testimony on this issue from each parties' expert. The testimony and cross-examination provided substantial evidence that the bits represented a format and together formed a bit string. Thus, the court finds that substantial evidence was presented for the jury to resolve the issue in favor of Broadcom.

In sum, the court finds that under the court's claim construction a reasonable juror could find the Flashtalk product embodied the TFSM structure and bit string representations of format sets. Thus, Intel's motion for judgment as a matter of law for validity of the '830 patent is denied.

V. INTEL'S MOTION FOR JUDGMENT AS A MATTER OF LAW FOR INFRINGEMENT AND DAMAGES OF THE '201 PATENT

The jury concluded that Broadcom's accused products did not infringe claims 1 and 10 of the '201 patent. As to claim 1, the jury found that the accused products lacked: (1) the pixel interpolating means; (2) the sequencing means; and (3) the arithmetic data processing means. As to claim 10, the jury found that the accused products lacked: (1) the arithmetic processing means; and (2) the means responsive.

A. Pixel interpolating means of claim 1

This is a means-plus-function element. The corresponding structure is subtractor 824, multiplier 825, adders 856 and 858, and two input registers, and structural equivalents. The structure must be responsive to a control signal.

Broadcom argues that the pixel interpolator of the accused devices do not use the structure identified in the court's claim construction. Specifically, Dr. Girod and Intel's expert, Dr. Von Herzen, agreed there is no subtractor circuit or multiplier circuit used. Rather, the accused devices use adders, shifters, and registers.

Dr. Von Herzen testified for Intel that one of ordinary skill in the art would consider the accused structures to be equivalent to the structure identified by the court, because the differences between the two are insubstantial. *See Odetics, Inc. v. Storage Technology Corp.*, 185 F.3d 1259, 1268 (Fed.Cir.1999) ("individual components ... of an overall structure that corresponds to the claimed function are not claim limitations. Rather, the claim limitation is the overall structure corresponding to the claimed function").

Dr. Girod testified that the structural differences between the two products were more than insubstantial and that one of ordinary skill in the art

would consider adder-based interpolators to be substantially different from the subtractor and multiplier-based circuit of the claim.

Intel bore the burden of proving structural equivalents. The jury was presented with substantial evidence that the structures of the accused devices were not equivalent to those of the claim.

B. Sequencing means of claim 1

The sequencing means performs the function of generating a control signal to condition the operation of the statistical decoding means, the arithmetic data processing means, and the pixel interpolating means to operate simultaneously. The components are required by the claim language to be responsive to (i.e., each component must be able to respond or react to) this control signal such that when the control signal is received, the component is put into a specified state. The corresponding structure of the sequencing means is the microcode RAM 310, instruction register 316, multiplexor 320, and a portion of the control block 308 that generates the LI and MXC signals, and structural equivalents.

***21** Broadcom presented evidence that its products do not generate the claimed control signal and do not include structures that are equivalent to the corresponding structures of the claimed sequencing means.

As discussed previously, the court found that substantial evidence supports the jury finding that the accused devices do not have the claimed pixel interpolating means. As the function of the sequencing means is "generating said control signal to condition ... said pixel interpolating means," the absence of the claimed pixel interpolating means indicates that the function of the sequencing means cannot be met. [FN7] Thus, solely on this basis, substantial evidence exists to support the jury's conclusion that the sequencing means claim limitation is absent as well.

> FN7. The same reasoning applies to the jury's finding regarding the arithmetic data processing means of claim 1. As the claim element includes the pixel interpolating means, substantial evidence exists that the element is not present in the accused products.

Broadcom further argues that Dr. Girod explained that the accused structures (7010 MB_Control and 7020 Row RISC) do not perform the function of generating the single control signal for providing instructions to the other components. He explained that the '201 control signal works "like an orchestra conductor" to coordinate all the devices, while the accused structures work "like a mailman" sending instructions to different components at different times. Finally, Broadcom asserts that numerous structural elements of the claimed sequencing means are absent from the accused structures such as a microcode RAM, an instruction register, a mux and a control block. Dr. Girod also concluded that the differences between the accused products and the patented structures were not insubstantial and that, therefore, the accused products are not equivalent to the claimed structures.

The structure of the sequencing means of claim 1 is the same as the structure of the control means of claim 10. They are essentially the same element by a different name. Intel's main argument on the sequencing means limitation is that the jury necessarily rejected Broadcom's argument because it "found the BCM 7010 and BCM 7020 include structure corresponding to the 'control means' of Claim 10[.]" (D.I. 756 at 34) Intel, therefore, believes the verdict is inconsistent.

One major problem with Intel's argument is that the jury made no definitive finding as to the control means. On the verdict form, the jury was not asked to check the elements that it found to be present in the accused products. The jury was only required to indicate the elements they found to be missing. The court cannot conclude from the verdict form, as Intel would like to assume, that the jury unanimously found any elements to be present in the accused products. The court only knows which elements the jury unanimously found not present in the accused products.

As to function, Intel contends that the court's construction does not require a single control signal, but only that each component respond to the same control signal, which Intel argues can be accomplished as the signal passes from one component to another. Broadcom asserts that the claim construction required one signal that coordinates the simultaneous operation of the components. Intel counters that the one signal could be pipelined through the elements.

***22** Intel argued throughout that the claim construction did not require one signal sent simultaneously to all components to be controlled.

The court agrees. Nothing in the claim construction requires one signal to be sent simultaneously to all components. The claim construction only requires the components to operate simultaneously. Broadcom's expert, Dr. Girod, agreed that all of the components operate simultaneously. (D.I. 707 at 2527--2528)

As to structure, the sequencing means and control means is a programmable logic structure (including the microcode RAM and sequencer circuitry). The accused devices have a hard-wired logic circuitry ("a state machine").

Intel contends that the "hardwired" 7010 MB_Control structure is equivalent to the structure identified by the court for the sequencing means. In response, Broadcom notes that while Intel's expert, Dr. Von Herzen, testified that the "hardwired" structure could be substituted for the claimed corresponding structure, this is insufficient to establish equivalence. *See* *Chiuminatta Concrete Concepts, Inc. v. Cardinal Industries, Inc.*, 145 F.3d 1303, 1309-10 (Fed.Cir.1998) (interchangeability does not establish equivalence); *but see* *Odetics*, 185 F.3d at 1268 (rejecting notion that *Chuminatta* requires a "component by component" equivalence test). In addition, Broadcom's expert, Dr. Girod, concluded that these structural differences were not insubstantial and that there was no structural equivalence.

The foregoing demonstrates that Broadcom provided substantial evidence that the accused structures did not contain equivalent structures to that of the sequencing means (or control means). The jury had substantial evidence to resolve this issue in Broadcom's favor. [FN8]

> FN8. Intel argues that the fact that sufficient evidence exists to support a finding of absence of the sequencing means claim element only with respect to the structure creates an inconsistent verdict. If the jury found the sequencing means structure absent, the jury should have found the structure for the control means claim element in claim 10 absent as well. Such an inconsistency is not an issue because as previously discussed, the fact that the pixel interpolating means claim element is absent is sufficient to support a finding that the function of the sequencing means claim element is absent.

C. Arithmetic processing means of claim 10

The corresponding structure of arithmetic processing means of claim 10 is adder 450 or adder 452, and one or more of the Boolean logic gates (such as OR, NOR, XOR, AND, or NOT) depicted in figure 4B of the '210 patent. The structure must be responsive to a control signal. The function is performing arithmetic and Boolean functions on binary values. Figure 4B is reproduced below.

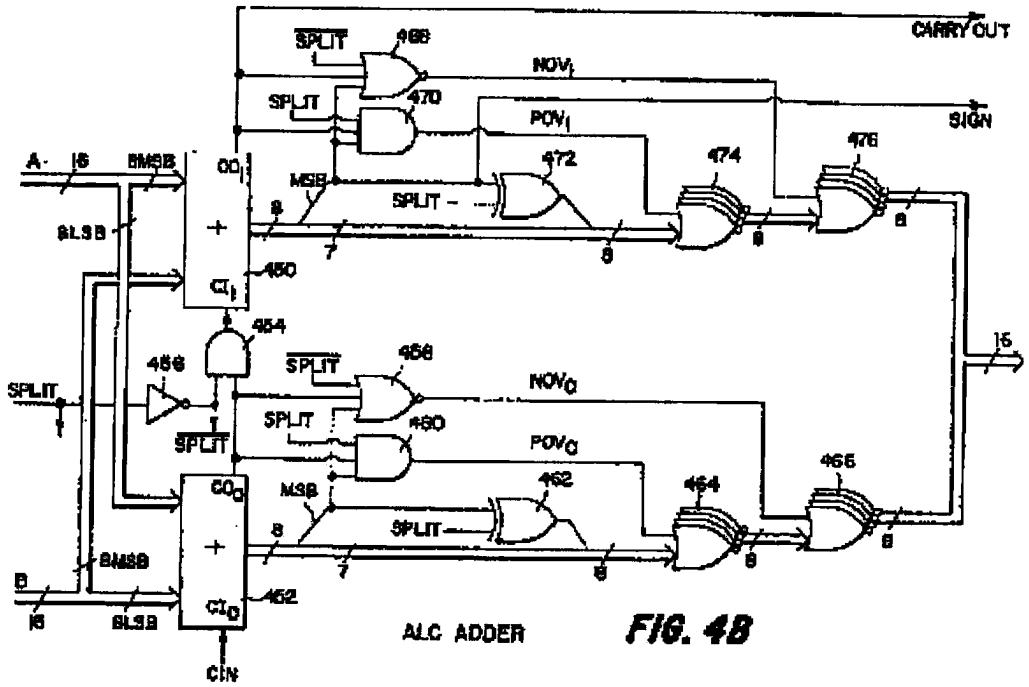

FIG. 4B

The court's claim construction requires that the arithmetic processing means performs both an arithmetic function (i.e., addition, subtraction, etc.) and a Boolean function (i.e., a logical function such as OR, AND, NOT, etc.). The arithmetic processing means must perform each of these two functions in response to the claimed control signals.

In its written contentions to the jury, Broadcom asserted that this element was not present because the Broadcom Differential Decoder and IDCT_ACC modules in the accused devices (the accused structures in the BCM 7010 and BCM 7020): (1) are incapable of performing a set of at least one arithmetic and at least one Boolean function; and (2) do not perform the required Boolean function in response to control signals.

*23 The accused structures in Broadcom's devices perform a function called "saturation" or "clamping," which takes values less than 0 and greater than 255 and sets them at 0 or 255. This ensures that all values are between 0 and 255 and can be digitally represented in binary.

1. Boolean Function

Broadcom's expert, Dr. Girod, testified that the accused clamping and saturation functions were not Boolean functions, but were arithmetic functions. He testified that while the accused structures are built using a series of logic gates, this, in and of itself, does not mean that they perform a Boolean function. (D.I. 707 at 2452) During closing argument, Broadcom accentuated the difference between having a logic gate (Boolean) structure and performing Boolean functions. Broadcom argued that the accused structures only perform arithmetic functions.

Broadcom's arguments regarding the lack of the Boolean function are against the court's claim construction. The preferred embodiment of the '201 patent itself includes an arithmetic processing means that performs the function of saturation. ('201 patent, col. 14, 11. 20-39) Therefore, it cannot be argued that the accused devices, which also perform the saturation function, do not meet the arithmetic processing means limitation, because the function of saturation is not Boolean. Furthermore, the court's claim construction states that "[t]o satisfy the function of performing Boolean functions a structure must be able to perform at least one of the Boolean operations, such as the AND operation, for example." *Intel*, 172 F.Supp.2d at 550. Broadcom admits that the accused devices contain Boolean logic gates such as AND/OR gates. (D.I. 707 at 2513) It cannot be argued that these Boolean logic gates do not perform Boolean operations. Based on the court's claim construction, performing at least one Boolean operation satisfies as performing a Boolean function. As a matter of law, the accused products perform a Boolean function. [FN9]

FN9. Broadcom's expert, Dr. Girod, appeared to misunderstand the law regarding means-plus-function claims. As a matter of law, the structure identified by the court must perform the function required by the claim. *See Asyst Tech., Inc. v. Empak, Inc.*, 268 F.3d 1364, 1369-70 (Fed.Cir.2001). Dr. Girod testified:
The Boolean functions that are required by the claim cannot be carried out by this circuit here in figure 4B. In fact, there is no structure, no circuit disclosed in the patent, that shows how to do that Boolean function.... The Boolean function that the claim requires is not shown in this figure 4B.
(D.I. 707 at 2509-10) However, as Intel points out, this is incorrect as a matter of law. Figure 4B contains the structure, as identified by the court, that performs the recited function. The structure identified by the court must perform the claimed function in a means-plus-function claim. *See id.*

2. Responsive to Control Signals

Broadcom also argues that the arithmetic processing means is not "responsive to control signals." Dr. Girod also testified that based on his review of the Verilog code, which describes the internal operation of the accused structures, the functions performed were not conditioned by (i.e., responsive to) control signals. (*Id.* at 2452-53)

Intel disagrees, concluding that "after finding the control means present in both the BCM7010 and BCM7020, no reasonable jury could have found that the arithmetic processing means is not responsive to control signals." (D.I. 756 at 25) As previously discussed, the jury was only required to indicate the claim elements they found to be missing. The court cannot conclude from the verdict form, as Intel would like to assume, that the jury unanimously found any elements to be present in the accused products. Thus, Intel has failed to carry its burden to prove that no reasonable jury could find the arithmetic means claim element missing from the accused products. [FN10] Intel's motion for judgement as a matter of law with regards to claim 10 of the '201 patent is denied. [FN11]

FN10. Both parties agree that the jury could only find the means responsive claim element absent based on finding the arithmetic means claim element absent. Thus, the means responsive claim element's presence or absence is tied to the presence or absence of the arithmetic means claim element.

FN11. As will be discussed, the fact that the jury found the arithmetic processing means claim element to be absent but did not find the control means claim element absent does create an inconsistent verdict and warrants a new trial on claim 10.

VI. BROADCOM'S MOTION FOR JUDGMENT AS A MATTER OF LAW THAT BROADCOM'S PRODUCTS DO NOT MEET THE CONTROL MEANS LIMITATION OF CLAIM 10 OF THE '201 PATENT AND INTEL'S MOTION FOR NEW TRIAL WITH RESPECT TO CLAIM 10

***24** In finding that Broadcom's accused products did not infringe claim 10 of the '201 patent, the jury specifically found that the elements which were not present were the arithmetic processing means and the means responsive. The jury did not check the box next to the control means element to indicate that it found that the control means element was also not present in the accused devices.

Broadcom has moved for judgment as a matter of law that its products do not meet the control means limitation of claim 10 of the '201 patent. The basis for its motion is that: (1) since the jury concluded that the accused products had no arithmetic processing means and the function of the control means is "to selectively condition ... said arithmetic processing means," it logically follows that the control means element cannot be satisfied because it cannot perform its function; (2) apart from that, no reasonable jury could find that the accused products have the required structures of the control means since the corresponding structures of the sequencing means and control means are identical. In response, Intel contends that Broadcom's motion demonstrates that the jury verdict is inconsistent and requires a new trial.

In its reply brief, Broadcom argues that the verdict is not inconsistent. Broadcom argues that "Intel attempts to manufacture an inconsistency by inferring that the jury made a finding nowhere present in the verdict form. Intel infers that by failing to check the box next to the control means, the jury must have unanimously found that the control means was present in the accused products." (D.I. 789 at 6) The

court, however, agrees that the fact that the jury did not mark the control means element as not present in the Broadcom products does not mean that the jury unanimously found that the Broadcom products include the control means element. Because the jury was only asked to make findings as to what was not present, it is improper to infer that the jury concluded that elements which were not checked off as not present were in fact present.

Two potential inconsistencies in the jury's verdict exist. One, the jury found the sequencing means to be absent in the accused devices, but did not find the control means to be absent. As previously discussed, this is explainable. Although these two elements share the same corresponding structure, they have different corresponding functions. One function of the sequencing means is to condition the pixel interpolating means, which the jury found to be absent. Since the jury found the pixel interpolating means absent, they may have reasonably concluded that the function of the sequencing means is not performed by the accused products. The control means, on the other hand, does not interact with the pixel interpolating means.

The second potential inconsistency is that the jury found the arithmetic processing means of claim 10 to be absent, but did not find the control means to be absent. This latter "inconsistency" is the one focused on by Broadcom in its motion.

***25** The function of the control means references and requires selectively conditioning the arithmetic processing means. If the arithmetic processing means is not present in the accused devices, the devices cannot perform the function of the control means. Thus, it logically follows that the control means (which as part of its function generates a code word that conditions the arithmetic processing means) cannot be present if the arithmetic processing means claim element is not present. The jury, however, not did reach this conclusion. In this regard, the jury verdict is inconsistent. The court cannot assume any set of facts to support the jury's conclusion that the arithmetic processing means claim element is absent and yet not find that the control means claim element is absent. The court agrees with Intel that this inconsistency illustrates the need for a new trial with respect to claim 10. Thus, Broadcom's motion for judgment as a matter of law with respect to the control means element of claim 10 is denied and Intel's motion for new trial with respect to claim 10 of the '201 patent is granted.

VII. INTEL'S MOTION FOR NEW TRIAL

Intel's motion for a new trial lists a number of evidentiary rulings by the court and statements/tactics by Broadcom that it contends unfairly prejudiced and tainted the proceedings. To prevail on its motion based on purported "misconduct," Intel must demonstrate both that Broadcom engaged in impropriety and that impropriety made it "reasonably probable" that the verdict was influenced by prejudicial statements." *Greenleaf v. Garlock, Inc.*, 174 F.3d 352, 363 (Fed.Cir.1999). The court will address each of Intel's arguments in turn. [FN12]

> FN12. Intel also argues it is entitled to a new trial based on the sufficiency of the evidence with regards to each claim asserted. The court has considered these arguments with respect to Intel's motions for judgment as a matter of law.

A. "This case is not about patents, it's about competition"

Counsel for Broadcom stated in his opening that "this case is not about patents, it's about competition." (D.I. 694 at 180) Seizing on this language, Intel contends that this language, and other language like it, improperly focused the jury on Intel's motives for filing the case, rather than the merits. Standing alone, this statement and others like it have nothing to do with whether Broadcom's products infringe the asserted claims of Intel's patents. The statements are facially improper.

However, immediately following that statement, another member of Broadcom's counsel stood up in his opening and stated that "I want to talk about patents because this is a patent lawsuit," and proceeded to explain why Broadcom does not infringe the '201 and '830 patents. (*Id.*) The jury instructions, witnesses, exhibits, closing arguments and written contentions to the jury focused exclusively on patent issues. Thus, Judge McKelvie was able to corral any attempts to focus on non-patent issues and force Broadcom and the jury to focus on the patent issues. Despite certain statements, when reviewing the whole case--the complex expert testimony and evidence on both sides regarding the patents, the accused products, and the prior art--it is impossible to conclude that the case was "not about patents."

B. The Dayna "Admission"

*26 The '830 patent was acquired by Intel from Dayna Communications. Part of the agreement that implemented the acquisition contained a warranty by Dayna that "no products infringe" Dayna's patents. Throughout trial, Broadcom argued that the legal effect of this provision was an admission by Intel that Broadcom's then-existing auto-negotiation products do not infringe the '830 patent.

Judge McKelvie precluded this argument, stating that "to the extent Broadcom is making arguments that the statement in the Dayna documents are an admission and have some legal significance, I don't agree. I think it's irrelevant." (D.I. 707 at 2719) Broadcom chose to argue this theory of its case, but was foreclosed from doing so (after many attempts) by Judge McKelvie. Intel never asked for a curative instruction on this, nor did Judge McKelvie issue one. Nothing about the admission was in the verdict form or jury instructions. Thus, the jury was properly focused on the legal determinations that it had to make.

C. The Intel/Broadcom Joint Development Agreement

This was the joint development agreement that Broadcom argued conferred a license for the '830 patent. The court ruled on summary judgment, that it did not. Intel complains that despite the court's ruling, Broadcom repeatedly referred to the agreement by stating that the auto-negotiation feature that Intel is complaining about was given to Intel by Broadcom. Judge McKelvie warned that those statements "sound like the license defense," and that "[i]f that's going to be a theme throughout the trial, we might as well shoot it now, because it's going to cause much more trouble than it's worth." (D.I. 696 at 455) Intel maintains that Broadcom continued to elicit testimony that alluded to the joint development project.

In response, Broadcom notes that it never argued to the jury that the joint development agreement conferred a license covering any of the accused products. But, as Judge McKelvie later noted, the fact that they had a joint development agreement, were cooperating partners, and that Broadcom may have thought it was licensed "may well be relevant to willfulness." (*Id.* at 457) This business relationship is also relevant to determining a hypothetical reasonable royalty rate for the purpose of determining damages. Cooperating partners are more likely to negotiate lower royalty rates. *See* *Georgia-Pacific Corp. v. U.S. Plywood Corp.*, 318 F.Supp. 1116, 1120 (S.D.N.Y.1970). Thus, the court allowed Broadcom to talk about the parties' commercial relationship.

Given that the agreement was relevant to damages and willfulness, Broadcom's reference to it was not unduly prejudicial. Similarly, facts regarding Intel's investment in Broadcom, which Intel accuses Broadcom of raising to show that Intel "milked" Broadcom, are relevant to damages.

D. Appealing to the Jury for Sympathy

Intel complains that Broadcom improperly appealed to the jury for sympathy, implying that a jury verdict in favor of Intel would "shut down" Broadcom and put Broadcom's 2700 employees out of work. Intel maintains that this is grounds for a new trial. *See* *Draper v. Airco, Inc.*, 580 F.2d 91, 95 (3d Cir.1978) ("jurors must ultimately base their judgment on the evidence presented ... there must be limits to pleas of pure passion"); *Hillard v. Hargraves*, 197 F.R.D. 358, 360 (N.D.Ill.2000) (where counsel implied defendants would have to pay for judgment against them out of own pocket, the court noted "improper references in closing argument are grounds for new trial").

*27 Broadcom responds that those statements were simply the truth--the case was important to Broadcom; its fate rested with the jury's decision. It argues that the "cumulative thrust" of its argument was a detailed review of the evidence in Broadcom's favor. *See* *Dorsett v. American Isuzu Motors, Inc.*, 805 F.Supp. 1212, 1219 (E.D.Pa.1992) ("All attorneys have an ethical duty to zealously advocate their client's cause," and courts do "not expect advocacy to be devoid of passion").

While some of Broadcom's allusions may have been overly dramatic, most of the statements were made during closing arguments to focus the jurors on the seriousness of the task before them when weighing the facts and evidence. Broadcom was not asking them to ignore those facts out of sympathy. Thus, these statements do not merit a new trial.

E. Attacks on Credibility

Intel complains that Broadcom attacked the credibility of its witnesses by insinuating that Intel paid for fact testimony. (e.g., "they paid him $200 an hour for testifying," "they paid him $150 an hour for his testimony," "He was represented by Intel attorneys at his deposition, because he's an Intel

employee and other than the salary, obviously, he's being paid by Intel for his testimony"). (D.I. 704 at 1860, 1866; D.I. 705 at 1897) After Intel objections, Judge McKelvie ordered Broadcom to stop its references to payment. Intel states that this was not sufficient, and that a new trial is warranted.

In response, Broadcom contends that these statements were neither erroneous nor prejudicial. It maintains that it did not mean to insinuate that the content of the testimony was paid for, but only that the witnesses were paid for their time and, thus, could be biased towards Intel.

When reviewing the whole case, the court finds that the jury was properly focused by the instructions and verdict form.

F. Admitted Evidence

Intel contends that the following evidence was improperly admitted: Mr. Huff's testimony, the TOPS article, testimony regarding non-disclosure before the PTO, and inventor deposition testimony. "In evaluating a motion for a new trial on the basis of trial error, the Court's inquiry is twofold: (1) whether an error was in fact committed, and (2) whether that error was so prejudicial that denial of a new trial would be 'inconsistent with substantial justice.' " *Finch v. Hercules Inc.*, 941 F.Supp. 1395 (D.Del.1996) (internal citation omitted). The court has reviewed Judge McKelvie's evidentiary rulings and finds no error was in fact committed. Even if any of the rulings were in error, Intel has failed to prove that denial of a new trial would be inconsistent with substantial justice.

VIII. INTEL'S MOTION FOR JUDGMENT AS A MATTER OF LAW AND MOTION FOR NEW TRIAL REGARDING BROADCOM'S THIRD-PARTY LICENSE DEFENSES

The court's final pre-trial opinion addressed Intel's motion for partial summary judgment concerning an Intel/Broadcom Joint Development Agreement and Intel and Broadcom's cross-motions for summary judgment concerning certain license defenses raised by Broadcom. *Intel Corp. v. Broadcom Corp.*, 173 F.Supp.2d 201 (D.Del.2001).

***28** These license agreements are relevant to one aspect of Intel's post-trial motions. The license issue was included in the verdict form and the "have made rights" license agreements were moved into evidence, thus becoming a jury issue despite the fact that Broadcom did not offer a witness to testify about them. As part of its verdict, the jury found for Broadcom on all twelve licenses included in the verdict form. The jury found that the above licenses gave Broadcom authority to sell its products to those twelve Intel licensees. Intel has moved for judgement as a matter of law and for a new trial that Broadcom is not licensed under these agreements.

Intel contends that the jury's conclusion that Broadcom's infringing activities were authorized under Intel's third party license agreements was unreasonable and completely unsupported by any evidence Broadcom offered at trial. First, the only mention of Broadcom's license defense in the entire trial came from Broadcom's damages expert, who simply testified that if Broadcom did have some sort of "have made" rights under the listed Intel third party licenses, Broadcom would owe Intel about one million dollars less in damages. Second, Broadcom failed to meet the threshold requirements for Broadcom's third party license defense that the court set out in its pre-trial opinion on the license defenses. Third, Broadcom offered no evidence that its accused products qualified as licensed products under each license. Fourth, in its opinion, the court had reserved judgment on Intel's assertions that many of the Intel licenses contained restrictive provisions (i.e., "Sanyo limitations"). Broadcom did not address these at trial.

In response, Broadcom states that the jury was properly instructed on the issue and that the agreements themselves were sufficient evidence for the jury to resolve the issue. Reading the agreements shows who is licensed and whether the license contains "have made rights." Also, Broadcom notes that the testimony of its Director of Financial Operations, Ray Vincent, stating that Broadcom does not manufacture a product until it receives an order for the product from a customer establishes the fourth requirement of the jury instructions that the products were not sold "off the shelf."

Jury Instruction 8.1 provided the jury with the elements Broadcom was required to prove to establish its license defense. Jury Instruction 8.1 reads in relevant part:

> An accused infringer may be protected from infringement liability if the accused infringer makes products for the use or sale of a licensee under a patent in suit. In order to take advantage of such "have made" rights, the accused infringer must prove the following factors:
> First, the accused infringer must prove that the party for whom it produces the accused product

was a licensee under the patent in suit at the time of the accused sales.
Second, the accused infringer must prove that the licensee has valid "have made" rights under its license to the patent in suit. For the licensee to have valid "have made" rights, the license agreement must authorize that licensee to have the patented product, or a portion of the patented product, made for it by an outside source like the accused infringer.
***29** Third, the accused infringer must prove that the products it makes are "licensed products" as defined under the license.
Fourth, the accused infringer must prove that it made products pursuant to a request from the licensee. If the accused infringer sells "off the shelf" or stock products, the accused infringer would not be protected from infringement liability under "have made" rights.
(D.I. 689 at 60)

The court finds that the jury's verdict with respect to the license issues is against the clear weight of the evidence. Most compellingly, the jury found that Broadcom had authority to sell products under the Intel/Dell agreement. The Intel/Dell agreement, however, was not submitted to the jury. Thus, the jury could not have reviewed the Intel/Dell license agreement. The jury's finding on this agreement cast doubt upon the jury's findings as to all of the third party agreements.

Furthermore, upon review of the record, the court is unable to determine any factual issue to be resolved by the jury. [FN13] Broadcom stated that the jury would be required to determine if the accused products fit the definition of the licensed products. (D.I. 708 at 2788) Broadcom, however, provided no evidence outside of the license for the jury to make such a determination. Contract interpretation is a matter for the court, not the jury. If the determination is to be made on the face of the license agreements, the court must decide this issue as a matter of law. Thus, the jury verdict regarding Broadcom's license defense is vacated and Intel's motion for new trial on the license defense is granted.

FN13. Judge McKelvie also noted his doubts regarding an issue of fact for the jury during the charge conference. (D.I. 708 at 2788)
The absence of a factual issue at trial is not surprising. In filing cross-motions for summary judgment on these licenses prior to the trial, the parties agreed that there were no disputed issues of fact--that the dispute regarding the scope and effect of the licenses was purely a legal dispute. In its opinion, the court did not reach the contract interpretation aspect of this issue, concluding instead that the facts were insufficient to demonstrate that the third party licensees conferred their authority to Broadcom.

IX. CONCLUSION

For the reason's stated, Intel's motion for judgment as a matter of law and motion for new trial on infringement of the '830 patent is denied. The court finds substantial evidence exists for a reasonable jury to find the transfer format selection means claim element absent. Intel's motion for judgment as a matter of law and motion for new trial on validity of the '830 patent is also denied. The court finds substantial evidence exists to find that the Flashtalk product anticipates the '830 patent.

Intel's motion for judgment as a matter of law and motion for new trial on infringement of claim 1 of the '201 is denied. The court finds substantial evidence exists for a reasonable jury to find the pixel interpolating means, the sequencing means and the arithmetic data processing means claim elements absent from the accused products.

Intel's motion for new trial on claim 10 of the '201 patent is granted. The jury verdict is inherently inconsistent and, thus, warrants a new trial.

Intel's motion for new trial on the license defense is granted. The court finds that the jury's verdict with regards to the license defense is against the great weight of the evidence. An appropriate will issue.

ORDER

At Wilmington, this 13th day of February, 2003, consistent with the opinion issued this same day;

IT IS ORDERED that:

***30** 1. Intel's motion for summary judgment as a matter of law (D.I.725) is denied.

2. Intel's motion for new trial (D.I.726) is granted in part and denied in part.

3. Broadcom's motion for judgment as a matter of law that Broadcom products do not meet the control means limitation of claim 10 of the '201 patent

(D.I.723) is denied.

2003 WL 360256 (D.Del.)

Motions, Pleadings and Filings (Back to top)

- 1:00CV00796 (Docket) (Aug. 30, 2000)

END OF DOCUMENT